Electronics Status

K. Einsweiler, LBNL

Next Steps for FE-D line:

- Discuss what are the next steps, how far should we proceed in our evaluation of FE-D2, do we prepare an FE-D3 and on what timescale, etc.
- Discuss steps for other chips in reticle (MCC-D2, DORIC2, VDC2).

Update on 0.25μ work:

- Status of FE-I effort, and schedule milestones

System Testing, Cables and Patch Panels, Power Supplies:

- Updates and hot issues

FE-D2 Evaluation

Steps towards complete FE-D2 evaluation:

- Complete wafer characterization of yield, and differences in yield for corner wafers of experimental run.
- Complete characterization of bare die, in terms of analog and digital performance of the design, looking for flaws.
- Irradiate single bare die on rad-hard support cards. Check the behavior during irradiation (SEU) and post-rad (total dose).
- Select good die, and have wafers bumped and assembled into bare modules. Make all standard lab and testbeam measurements of performance.
- Perform irradiations of single chip and 16-chip flip-chipped module assemblies. Look for additional performance issues during and after irradiation.

Steps towards production version of FE-D:

- Next step would be to compile a list of necessary modifications to address whatever issues arise in the evaluation, and then proceed towards an FE-D3 submission, which would be a “pre-production” version of the FE chip.

What have we learned so far from FE-D2 testing

For FE-D2D:

- Observe that known digital problems (buffer sizing, etc.) seem to have been properly fixed.
- Observe similar yield and readout problems to those seen in FE-D1b (backup) run. This means that there are many columns which fail because of “Row 0” problems. The yield of the Pixel Register is similar to FE-D1b. The yield of chips with nine good column pairs is typically 0 per wafer, with at most a few such die per wafer. In all of the FE-D2 probing at LBL so far, there has not been a single “digitally perfect” chip (all pixels in all column pairs working with digital injection).
- There is no apparent (strong) correlation of FE-D2D column-pair yield with the processing corners in the experimental run. This suggests that we continue to have no clues about how to improve this unacceptable yield.
- Just as with FE-D1, because of the severe readout problems in every chip, it is very difficult to get stable analog performance from a single chip. It does not seem useful to make any modules with these chips.

Conclude: this design in DMILL seems to be a dead-end...

- The one possible exception to this is that ATMEL has a theory that defects in the base wafers could be a source for our problems (and SCT yield problems), so they plan to do an experimental run with new wafer supplier in the near future.

For FE-D2S:

- The yield for the digital readout is much better than for the FE-D2D chips. If one uses the loose critieria that a good die has good registers and nine good column pairs (allowing a small number of dead pixels per good column pair), then the yield is about 50%. There are typically a few bad pixels per chip in this sample.
- See only two yield issues correlated with corners. The first is that for large Leff, the Pixel Register yield is reduced. The second is that for small Leff, the number of bad pixels in good column pairs is increased. Since this particular variation is a mask change, and has electrical consequences for device speed, these may be legitimate indications of marginal aspects of our design.

Conclude: this design works well enough to justify further evaluation.

Comments on Wafer Probing:

- First comparison between Bonn and LBL wafer probing was carried out in the last few days. Example results show generally excellent agreement:

	GLOBAL REGISTER	PIXEL REGISTER		GOOD COLUMN PAIRS		PERFECT COLUMN PAIRS		MEAN BAD PIXELS
WAFER	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER GOOD CHIP*
03								23/18 = 1.3
	40/40	349/360	34/40	299/349	18/34	244/349	3/34	
LBL	100%	97%	85%	86%	53%	70%	9%	
	40/40	349/360		315/349		242/349		
BONN	100%	97%		90%		69%		
04								33/23 = 1.4
	40/40	356/360	37/40	319/356	23/37	282/356	12/37	
LBL	100%	99%	93%	90%	62%	79%	32%	
	40/40	356/360		329/356		284/356		
BONN	100%	99%		92%		80%		
09								94/15 = 6.3
	39/40	348/351	36/39	262/348	15/36	212/348	2/36	
LBL	97%	99%	92%	75%	41%	61%	6%	
	39/40	344/351		305/344		224/348		
BONN	97%	98%		89%		64%		
10								54/11 = 4.9
	38/40	298/333	26/38	224/298	11/26	181/298	1/26	
LBL	95%	90%	70%	75%	42%	61%	4%	
	38/40	294/342		216/294		164/294		
BONN	95%	86%		73%		56%		

Comments on overall chip performance:

- The peculiar analog behavior seen in FE-D1 is unfortunately confirmed in FE-D2. The results of threshold scans are seen to fluctuate from scan to scan when hard resets are performed. In addition, there is a significant left-right asymmetry in the average threshold, which does not correlate with the measured values of VCCD and VTH on the two sides of the die, and leads to dispersions of about 600e.
- There is sometimes a lack of reproducibility in the digital injection results. Occasionally, one sees many consecutive rows of pixels in which the hit efficiency is only 50% or 75%. This effect is greatest at 20MHz column clock speed, and is fairly minimal at 5MHz column clock speed.
- There are some indications that the noise performance continues to be worse than expected in the complete arrays, but is quite reasonable in the Analog Test Chip. This was seen to show up most dramatically with FE-D1 in the bumped assemblies, and appeared to be correlated with clocking of the digital readout logic. It was not reduced by back-side plating in FE-D1, nor (apparently) by improved guard ringing and input pad shielding in FE-D2.
- These problems are seen in both FE-D2S and FE-D2D, and were seen in FE-D1. Therefore, they cannot be related to the readout oscillation problems observed in FE-D2D and FE-D1.
- We should make an effort to understand them, in case they arise from a generic design flaw (which could in principle re-occur in future chips in other processes).

Summary Comments on FE-D2:

- The present FE-D2D design seems to be useless for further investigations, due to the very poor yield for useful chips, and the very unstable operation of those chips that do work. We have no idea how to fix these problems at this time. This is the only design we know of that allows us to fit the desired functionality into a 50μ x 400μ pixel in DMILL.
- The present FE-D2S design looks promising in terms of its yield, but the pixel is completely full. Additional space would still need to be found to re-introduce the 3-bit TDAC into the pixel, and the large dispersions we observe in FE-D2S desperately need this trim capability.
- It seems likely that the only way to implement an FE-D3S would be to increase the size of the pixel beyond 400μ, perhaps to 450μ to give a safety margin (16 column pairs per chip) in the layout.

Two choices:

- Go ahead with an FE-D3S with a larger pixel geometry.
- Continue to emphasize FE-I and return to create an FE-D3 only if there are indications of serious problems with the 0.25μ design.
- Clearly favor the latter direction...

What do we know about die from FE-D1 run ?

- Irradiations of VDC-D1 showed successful operation after 50MRad irradiation at the PS. There were problems with the operation of the LVDS I/O drivers, most likely related to the current reference circuit. After annealing, these problems disappeared.
- Irradiations of MCC-D0 provided measurements of SEU effects, and demonstration of proper operation during irradiation. All 8 devices irradiated were still working after 30 MRad. Some indications of SEU problems that affect LVDS I/O during operation (occasionally a given chip stops communicated, but can be restored to operation by resetting or power cycling). The rate of this (rare) occurrence could be consistent with SEU effects in the current reference required for operating the LVDS I/O blocks.
- Subsequent testing at Genova showed several devices no longer worked. The pattern of failures is not yet understood, and further study is underway.

What do we know about other die on the FE-D2 run ?

- Due to delays in getting hot wafers shipped to Bonn, etc, the first such wafers arrived only 2 weeks ago in LBL. One was quickly diced and parts distributed:
- All test chips from Bonn (Analog Test chip, Cap Test chip, Delay Test chip) work properly, and provide useful results.
- New VDC (essentially identical to the design in the FE-D1 run) and DORIC have been tested in a preliminary way by OSU, Siegen and Wuppertal. All groups confirm that new VDC works, and OSU/Siegen agree that new DORIC works.
- OSU has already begun BER measurements of a complete opto-link using the new DORIC, and comparing them with the performance of DORIC4A from SCT. The Pixel DORIC (DORIC-D2) works well, but seems to have a significantly higher noise (requires much more light on PIN diode to produce an acceptable BER). The observed performance is barely compatible with the expected light output from real links (which has large dispersion due to high precision requirements on mounting of VCSELs in opto-package). Further study of the DORIC-D2 chip is needed to see if this result is confirmed.
- A total of 19 packaged MCC-D2 have been delivered to Genova, but they arrived too late for testing before this meeting. They will be tested soon with the MCC exerciser in Genova, and then some will be sent to LBL to allow upgrading of PLL support for new command and data formats.

Next Steps for FE-D2 Chips

- Continue to study FE-D2S die in detail in the lab, including also the Analog Test Chip, in order to understand the performance of the design in detail, and make sure there are no mysteries that could come back to haunt us in future chips.
- Prepare single FE-D2S die for irradiation. We hope to do some first irradiations at LBL in Feb. We should go ahead and do this at the PS in April also, to make sure that we really understand how to do these irradiations.
- Perform thorough testing of MCC-D2. Characterize also a modest number of bare die for module construction. If all goes well, would expect to perform irradiations of MCC-D2, similar to those done this year for MCC-D0.
- Continue characterization of DORIC-D2 and VDC-D2, particularly noise performance of DORIC. Would then expect to irradiate chips and complete optical links based on VDC-D2 and DORIC-D2 at the PS this year.
- Send FE-D2 wafers for bump-bonding. Agreed to send three wafers each to AMS and IZM in January and build single chip and 16-chip modules with preproduction sensors. Other useful parts would be diced from these wafers (MCC-D2, DORIC-D2, VDC-D2). Should get roughly one module per wafer with some safety factor.
- Perform irradiations on complete single chip assemblies and complete module assemblies. Although the chips may not be perfect, and we may not make any additional chips with this vendor, still many things to be learned. The only route for qualifying pre-production sensors (requires irradiation) as well.

Proposed workplan:

FE-D2:

Carry out evaluation of FE-D2S devices as proposed, but try hard not to divert any IC design resources from FE-I effort.

DORIC-D2 and VDC-D2:

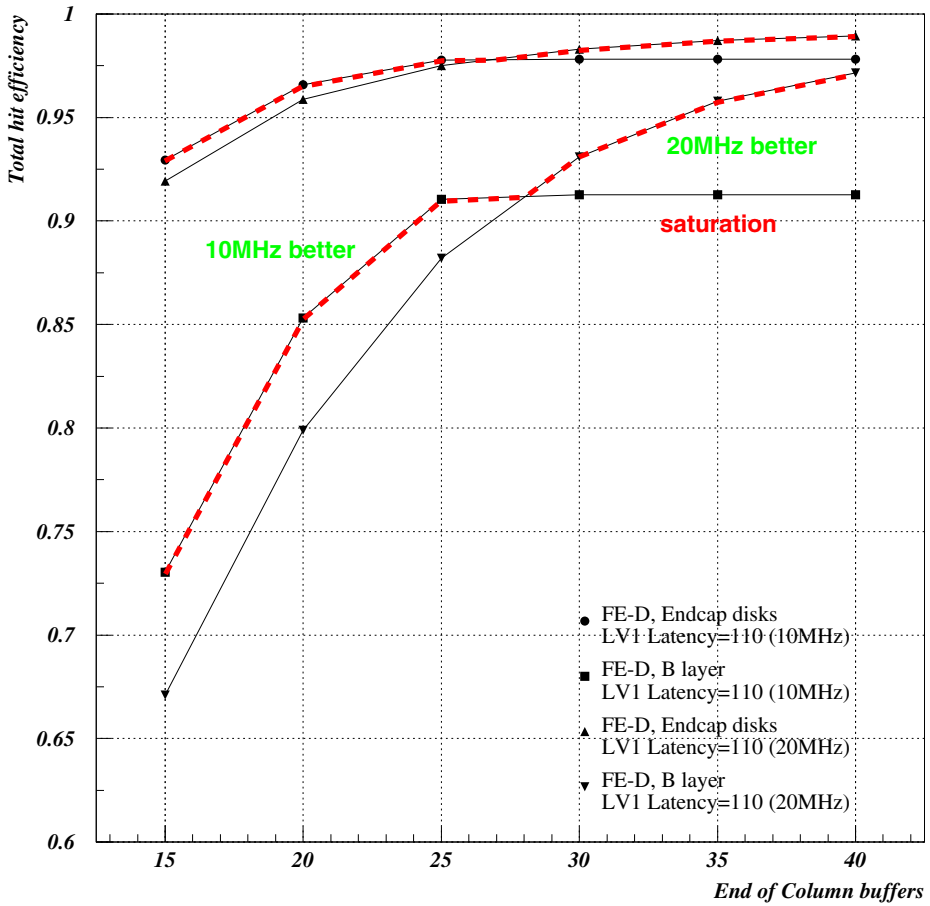
Make full evaluation of DORIC-2D and VDC-2D to see if they can serve as the basis for our optolinks. As a minimum, we should build significant number of optolinks and learn as much as possible about them. Carry out 0.25μ design work as well, but emphasize evaluation of present chips.

MCC-D2:

Make full evaluation of MCC-D2 performance, both in packaged form, and in bare die form mounted on some of remaining FE-B modules. Basic evaluation needed to validate design for MCC-I as well. Decide no later than Feb whether to continue emphasizing MCC-D line or to prepare MCC-I for submission on FE-I run. Cannot do both...

Goals of FE-I Design

- Start with geometry and buffering achieved in the HSOI design of 400μ pixel and 32 EOC buffers. New design should work at 2.0V for extra margin, and would start from FE-H pinout.
- Design copes with needs except for B-layer point resolution (300μ pixel preferred) and high efficiency at high luminosity for the B-layer (more buffering needed).



Study of D. Calvet indicating expected efficiency for hits (not clusters) versus number of buffers and column clock frequency.

Four basic sources of loss are: analog (TOT deadtime), digital (pixel readout busy), buffering (no free EOC buffer), and fakes (hits arriving in EOC too late for L1).

For 20MHz and 32 buffers, dominant source is available buffers, and this can be improved by increasing the buffer count still further to about 40.

Necessary changes for 0.25μ conversion include:

- Revised front-end design driven by lack of small W/L NMOS devices for enclosed layouts, and reduced supply voltage. Most likely requires different leakage compensation scheme and two-stage design, possibly providing better timewalk.

Basic improvements planned for design include:

- Improved threshold control with replacement of V-DACs and possible trimming of feedback current at pixel level for improved TOT and timewalk performance.
- Improved SEU tolerance of configuration registers and logic blocks.
- Fully static design of all logic and storage blocks for improved leakage and SEU performance (and possibly yield).
- Improved performance of pixel RAM and sense amplifiers.
- Improved robustness of basic logic blocks in readout path (pixel hit logic, CEU logic, EOC logic) via more synchronous state-machine-based designs.
- Increase number of TSI bits from 7 to 8 for increased latency range (even number of bits is natural in the layout).

More ambitious improvements to investigate:

- Investigate differential front-end design for improved common mode immunity.
- Investigate possibility of computing TOT in CEU and applying simply timing correction for timewalk at this stage.

Test Chip Program

Take advantage of frequent runs, rapid turnaround of TSMC:

- Earliest date for useful submission is Jan 8, with expected return of Mar 19.
- Goal of the initial submission is to include several of basic blocks from FE-I, and evaluate their performance.
- Gives opportunity to check that we understand design rules, that performance agrees with SPICE, and that behavior during irradiation (SEU) and post-rad (total dose) is as expected.

Present list of blocks includes:

- Current reference and current DAC used in bias control
- Redesigned LVDS driver and receiver blocks
- Prototype of new preamplifier design with leakage injection and capacitive loads
- Pixel RAM block with sense amplifier readout
- Several basic shift registers, for evaluation of SEU performance. Designs will include: standard cell version, SEU-tolerant version from CERN and Bonn, and three-fold majority logic version.
- Grey generator which has been synthesized and automatically placed and routed.

Progress towards submission on Jan 8 date looks good.

Next step should be more complete test chip:

- This would naturally be something like the Analog Test Chip included in FE-D runs. This included several short column-pair arrays of preamp/discriminator and bias circuitry, with all adjustment DACs and calibration circuitry, and real layout.
- It would allow us to demonstrate that the front-end design and all of the analog blocks intended for FE-I do indeed behave as expected.
- A submission on Feb 5, with return about Apr 16, would allow time to evaluate the results and make minor adjustments to the design if needed. If more significant issues were uncovered, the engineering run would have to be delayed.

Milestones in overall schedule:

- Schematics should be largely completed by early February
- Layout should be largely completed by early March
- Simulation and verification would then have almost three months to complete
- Submission would be June 1. In order to get the guaranteed turnaround, the design would need to be DRC-clean, requiring us to begin foundry-level DRC checking (using Hercules) at least several weeks earlier.
- Worst case thirteen week turnaround in the frame contract would give wafers during the first week in September. This might allow some testbeam and irradiation studies at CERN before shutdowns in early November...

Multi-Module System Tests with remaining FE-B Modules

- Many critical issues to explore that cannot wait until we have good FE-I modules in one year. We should learn as much as possible about Flex2, and power distribution/grounding/shielding problems from the best modules we know how to build today (FE-B/IZM). Of course, some things may change with final chips.

First: Fully test single Flex2 modules mounted on real thermal structures in LBL, Bonn, and Genova. All modules so far have been operated with supporting PC boards and Aluminum support plates. There could be some surprises...

Second: Complete sector assembly using one AMS module that we have in LBL already, and one additional FE-B IZM module that hope to get soon from Bonn. Imagine there will be similar stave efforts at Bonn and Genova.

Initial readout will be awkward, requiring the use of several PLL's. Plan to investigate minor modifications to PixelDAQ to support operation of multiple PLL (one at a time).

Third: develop simple BOC-replacement for ROD, to allow connection of several modules via copper cables (instead of opto-links). This would also provide critical user feedback to evolving ROD design, which should occur on timescale of Summer 2001.

Additional issue: We should build as many of these modules with MCC-D2 as possible, assuming that it works well. This requires delivering tested MCC-D2 die early next year, and requires PLL firmware upgrades as soon as tested, packaged parts are available from Genova (will exercise MCC-D2 with good bare module at LBL to test).

Cable Plant Definition

Many recent developments:

- We need to finalize connectivity and modularity of system. Many prototypes are underway, but the system design is still evolving, causing lots of wasted efforts...
- Reduce modularity of opto-link power supplies and controls (VVDC, VPIN, VISET, RESET) for half-stave or sector opto-board approach ? Seems to be the only viable approach to integration with the new squeezed layout.
- Implement voltage sensing down to module level ? Seems to be only conservative approach to large ΔV cable system. Proposal adds 3 small wires per module. This requires updating the pigtail design, the PP0 design, and pigtail connector pin count. If we want to propagate the sensing down to the lowest level (onto the Flex), also requires updating barrel elbow design, and Flex design. Example: new sense wires requires moving to 36-pin Elco connector (11.2mm width); new 8-sector disk allows tab width on Flex to increase to 12mm, so OK...
- Have updated ΔV allocations for cables to try to meet constraints in PP2 region. Total drops now 0.6V to PP0, 0.5V to PP1, 0.15V to PP2, 0.5V to PP3. Suggests again that we consider using rad-tol regulators at PP3. Will look at this more carefully over next few months, and see if it looks viable for us...
- Need better overall coordination and documentation of this critical area, which cuts across many parts of the pixel detector design.
- We should aim for a coherent and documented design for Feb. Pixel Week.

Summary of Action Items for Grounding/Shielding

- Critical driver for cable cost is maximum allowed ΔV and total cable length. If ΔV can be increased from 2V up to 3-4V, very substantial savings could be found. If half of supplies can be moved to US15, cable runs can be shortened significantly. Should re-consider implementing supply sensing up to module connection. This requires better understanding of grounding scheme, transient behavior of power supplies and electronics, plus transient protection scheme prototyping.
- Need to perform electrical characterization of carbon-carbon in Stave/Sector prototypes and carry out detailed electrical modeling of fully populated structures.
- Need to make sure that evolving beampipe design provides best Faraday cage possible within other constraints, and includes proper electrical contact points.
- Need to include appropriate metalization of new Support Tube in design to be sure we provide a low-impedance shielding and shunting path for noise currents.
- Need to begin multi-module system tests as soon as possible to investigate whether shunt-shields between modules and support structure are needed. Also need to further explore how module attachment would be modified if shunt shield is needed, back-side chip connection is needed, or both.
- Need to prototype different grounding schemes for pigtails and PP0, with full length power cables. Of particular concern is the case of barrel modules whose services run out in opposite directions from the detector, where the loop area of the services bundles is very large. The performance may depend critically on whether or not electrical isolation can be achieved between the two stave halves.